Masaaki NIWA Ph.D.

実用化開発を含むロジック用先端 CMOS のゲートスタックなどフロントエンドプロセスと MRAM 用磁気トンネル接合素子(MTJ)の極薄絶縁膜の原子レベルの界面制御、物理解析や信頼性物理などデバイスの材料物性関連の研究開発に従事してきました。

これまで培った電子デバイス用極薄誘電体膜に関する技術を通して、未知なる次世代 3D 積層技術の開拓に挑戦中です。

I have been mainly engaged in the Research and Practical development of Front-End-Process and Materials focused on gate stack of Advanced logic CMOS and Magnetic tunnel junction (MTJ) for MRAM including Atomic-scale interface control, Physical analysis and Reliability physics of Ultra-thin Dielectric films.

Currently, I am taking the challenge of unknown next-generation 3D-Stack technology through these potential technologies cultivated so far.

■ 1980– Matsushita Electric Industrial Co. Ltd. (currently Panasonic)

After development of impurity level measurement and formation process of photoconductive films (Chalcogenide amorphous semiconductor、Polycrystalline oxide) for image sensor, Dr. Niwa mainly engaged in the development of Advanced CMOS FETs in charge of R&D of Front-End-Processes focusing on 65-32nm CMOS gate stack process, Interface control, Physical analysis, and Reliablity physics.

▶ Until early 2000: **Basic study of ultra-thin gate oxide for advanced CMOS**

- 1990–98: Engaged in atomic-scale planarization of SiO_2/S (001) interface (Joint research with Stanford Univ.) and its analysis aimed at improving channel mobility based on interfacial morphology and breakdown voltage of MOS FETs.
- 1992 – 95: By means of self-developed Ultra-high Vacuum-Scanning Tunneling Microscope (UHV-STM), he focused on initial oxidation mechanism clarification such as atomic-scale observation of oxygen adsorption phenomenon on Si (001) surface. (Joint research with the Univ. of Tokyo)

  Meanwhile, he served as a *visiting professor at Kanazawa University* in charge of “VLSI Process Technology”.
- 1999–04: *Visiting researcher at STARC* * under Prof. M. Oshima (Univ. of Tokyo) on "Ultra-high resolution analysis of insulating film/silicon interface and breakdown reliability by Synchrotron radiation”

  STARC* : Semiconductor Technology Academic Research Center Inc.
- 2000–02: Started MOS operation and reliability verification of high dielectric constant insulating film (ZrO_2, HfO_2) as an alternative material to gate SiO_2 which has reached the limit of ultra-thinning. (Joint research with Univ. of Texas, Austin (UTA))

▶ Since 2002: **Practical development of logic CMOS with High-k gate dielectric (Chief Engineer, Councilor)**

- 2002–07: He proposed joint research with imec (Belgium) on advanced CMOS and was stationed at imec as an on-site manager of R&D of High-k / Metal gate system for 32nm-CMOS.

  Meanwhile, he served as a *visiting professor at the University of Leuven (KU Leuven)* in charge of “Nanoelectronics” as well as jury member of doctoral dissertation.

※ The 32nm-CMOS equipped with High-k / Metal gate system developed with imec has come to fruition as the world's first mass production of ultra-low power consumption system LSI for Blu-ray Disc players in 2010.

■ 2011– Worked at Universities (Univ. of Tsukuba, Tohoku Univ.)

▶ 2011−13: **Professor of Applied Physics Dept. at Graduate School of Pure & Applied Science, University of Tsukuba**

・Engaged in research on Power MOS, lectures on Nano-electronics including Human resource development as well as TIA* nano-project promotion (General manager of TIA Promotion Office)

TIA* : Tsukuba Innovation Arena

▶ 2013−20: **Professor of Research and Development Gr. of Center for Innovative Integrated Electronic Systems (CIES), Tohoku University**

・Engaged in materials science of Magnetic Tunnel Junction (MTJ) for STT*-MRAM elucidating the relationship between MTJ structure and characteristics. In particular, he focused on physical analyses of ultra-thin MgO / CoFeB interface and B behavior by hard X-ray photoelectron spectroscopy (HAXPES*) @ SPring-8*, as well as structural analysis of fine MTJ by means of co-developed electron tomography (STEM*-Tomography) combined with Scanning TEM.

STT*: Spin Transfer Torque
HAXPES*: Hard X-ray Photoelectron Spectroscopy
Spring-8*: Super Photon ring-8 GeV (Synchrotron radiation facility)
STEM*: Scanning TEM

In addition, he was responsible for execution of the JSPS* Core-to-core program (Advanced research network btw Tohoku Univ. - Cambridge Univ. - Paris-Sud Univ.)

■ Has been incumbent since 2020 (The Univ. of Tokyo)

▶ 2020−: **Senior Fellow at Advanced Device Research Gr., Systems Design Lab (d.lab), Graduate School of Engineering, The University of Tokyo**

- In charge of project management of NEDO* project on" Post 5G Information and Communication Systems Infrastructure Reinforcement R&D Project/ Advanced Semiconductor Manufacturing Technology/ Development of Direct Bonding 3D Stacking Technology (Equipment and Process Development for WoW and CoW)".

NEDO* : New Energy and Industrial Technology Development Organization

▶ 2023−: **Technical Advisor, imec**

▶ 2024−: **Visiting Scholar, Institute of Physical and Chemical Research**

Others;

◆ Activities on various academic societies, associations, and journals

・General chair of VLSI Technology Symp.

・IEDM Executive Com. (Asian Arrangement Chair) & Sub-com. member

・IRPS Device Dielectric com. Chair

・IEEE Technical Field Award (Cledo Brunetti Award) com. Chair

・IEEE EDS Japan Chapter Chair

・IEEE Fellow Evaluation com. Vice chair

・IEEE Semiconductor Interface Specialist Conference (SISC) com. member

・VLSI Symp. Executive Com. Member

・ITRS* - FEP* sub-com. member as Japan's national team

ITRS*: International Technology Roadmap for Semiconductors
FEP*: Front-End-Process

・STRJ* / JEITA*- FEP sub-com. Associate leader in charge of ITRS

STRJ*：Semiconductor Technology Roadmap Committee of Japan

JEITA*：Japan Electronics and Information Technology Industries Association

・MRS Symposium Organizer (High-k Dielectric)

・Appl. Phys. Lett Paper Review com. member

・External member of Senior Research Professor Evaluation com., KU Leuven

- External member of Flanders State Government-Foundation for Scientific Research Belgium/ New Research project Evaluation committee
- External evaluation com. member of Science and Engineering area of Kanazawa University

・External member of Tsukuba University's pre-strategy initiative field-specific evaluation com.

・Kyoto Prize Nomination com. member

・Member of NEF (Next Einstein Forum: Sponsored by African Institute of Mathematical Sciences (AIMS))

・Chairman of NEDO-Advanced Semiconductor Expert Committees

In addition, he has served as a member of various committees including the Japan Society of Applied Physics (JSAP) , the Institute of Electronics, Information and Communication Engineers (IEICE) and the Japan Society for the Promotion of Science (JSPS) and other international conferences.

◆ Fellow

- **IEEE Fellow** (2013)

"CMOS technology using high dielectric constant materials and metal gate"

- **JSAP Fellow** (2014)
  "Materials Research on Advanced CMOS Gate Stacks and Their Practical Implementation“

◆ Degree

- Ph.D. (Applied Physics) from Osaka University (1994/10)
  “Study on the Interfacial Atomic Structure and Electrical Properties of the Silicon-Thermal Oxide System”

- M.Eng. (Electrical Engineering) from Kanazawa University (1980/3)
  “Optical Modulation Mechanism Using CdS Acoustic Domains and Its Device Application”