# Biography
# Achievements & Accomplishments

Updated on 25 Apr 2022

**Dr. KAWANO Masaya**

*Project Researcher*

*Systems Design Lab (d.lab), The University of Tokyo*

# Biography

**Kawano Masaya** received the B.S. and M.S. degrees in nuclear engineering from **Osaka University**, Japan, and the Ph.D. degree in electronics and applied physics from **Tokyo Institute of Technology**, Japan, in 1987, 1989, and 2008, respectively.

In 1989, he joined **NEC Corporation**, Tokyo, Japan, where he was involved in cutting-edge research in the areas of infrared image sensors, Cu/low-k BEOL integration, and advanced packaging technologies for 22 years. He was with **EV Group Japan** from 2011 to 2015 where he worked on wafer bonding, nanoimprint lithography for 3D ICs, image sensors, LED, MEMS applications. He was with **Institute of Microelectronics (IME), A*STAR**, Singapore, from 2015 to 2021. He was a Senior Scientist with Heterogeneous Integration department where he was working on wafer-to-wafer/chip-to-wafer hybrid bonding, TSV and FOWLP technologies. He joined **the University of Tokyo** in 2022, and he is currently working on new project initiation of 3DIC and Advanced Packaging Material projects.

Dr. Kawano has authored and co-authored more than 20 peer-review journals, and has more than 60 US patents granted. He has been invited to give talks and lectures at various international conferences and workshops. He is also the recipient of IEEE EPTC Best Interactive Paper Award in 2017 and IEEE ESTC Best Paper Award in 2010 for the works on FOWLP, and won 13th SEMI Technology Symposium Award in 2006 for the work on Stacked-Chip Memory.

# Executive Summary of Research Topics

1989～1998

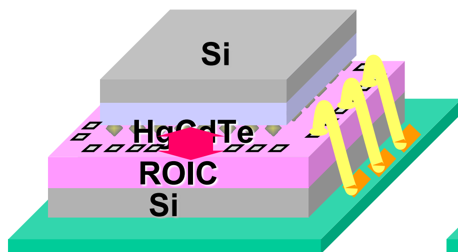
2003～Present

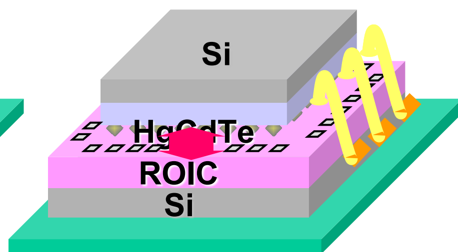
IR Sensor

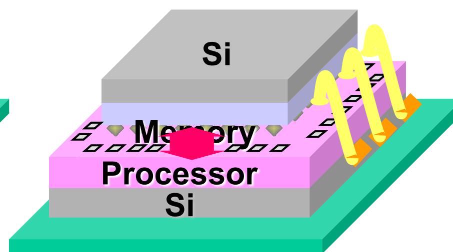
GMR Sensor

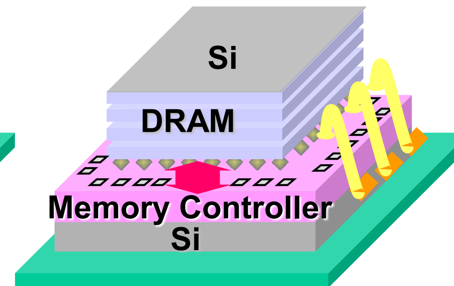
CoC

3D-Memory




HgCdTe/Si Hetero-epi

Evaluation of crystal defects

IR sensor operation

Magnetic sensing mech.

Cal. of Sensitivity

Molding Package

1998～2003

Cu/low-k integration

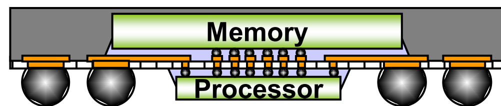
Cu/low-k process release

2009～2011

Bump line launch

CoC product launch

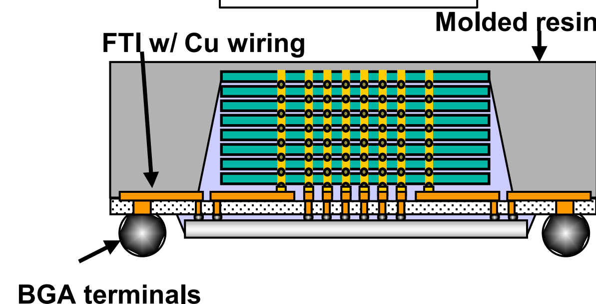
HD FOWLP




High-density bonding

High data-rate transfer

Multi-Chip Stack

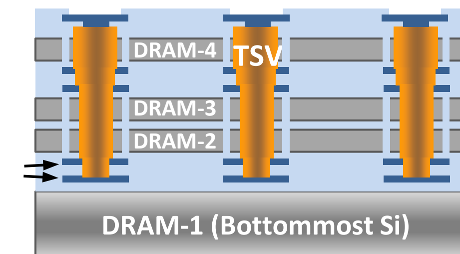



Through Si Vias

3D Assembly

Write/Read Operation

Multi-Wafer Stack




One-step TSV

Fusion Bonding

Hybrid Bonding

# Summary of Research Area (Advanced Packaging)

Plated Bump

RDL

Wafer-level BGA

Fan-out Rerouting

Fine-pitch bonding SiP

Multi-layer stack (Chip-stack/Wafer-stack)

Thick Cu wires

Fine-pitch bond

500 µm

Chip-stack w/ TSV

WLBGA

Fan-Out WLP

HD FOWLP (SMAFTI)

3D Stacked Memory

# Selected Papers

東京大学
THE UNIVERSITY OF TOKYO

RaaS

1) M. Kawano et al., 4 publications relating to “Wafer stacked 3D Memory with One-step TSV,” ***ECTC 2019, ECTC 2020, ECTC 2021, ECTC 2022*** (to be published).

2) M. Kawano et al., “Ultrathin Die Pick-Up for 3D Chip Stacking,” ***EPTC 2019***.

3) M. Kawano et al., “High Density TSV-Free Interposer (TFI) Packaging with Submicron Cu Damascene RDLs for Integration of CPU/GPU and HBM,” ***ECTC 2018***.

4) M. Kawano et al., “A novel temporary bonding and debonding technology for TSV fabrication and 3D integration,” ***J. Inst. Elect. Commun. Eng.***, Vol. J95-C, No. 11, pp. 439-446, Nov. 2012.

5) M. Kawano et al., "A 3-D Packaging Technology for Stacked DRAM with 3 Gb/s Data Transfer," ***IEEE Trans. Electron Devices***, Vol. 55, No. 7, pp.1614–1620, Jul. 2008.

6) M. Kawano et al., “HgCdTe and CdTe$(\bar{1}\ \bar{1}\ \bar{3})$B growth on Si(1 1 2)5° off by molecular beam epitaxy,” ***Appl. Phys. Lett.*** Vol. 69, pp.2876-2878, Nov. 1996.

**Peer-Review Papers**: 6 (First author), 14 (Co-author)

**International Conferences**: 16 (First author), 21 (Co-author)

**Google Scholar**: Citations: 2166, h-index: 25, i10-index: 56
https://scholar.google.com/citations?user=K07NglAAAAAJ&hl=en&oi=sra

# US Patents (65 granted)

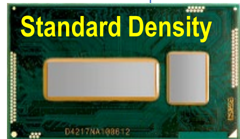
65) 10,720,339 Fan-out wafer-level packaging method and the package produced thereof
64) 10,580763 Electronic device
63) 9,978,512 Circuit device
62) 9,847,325 Electronic device
61) 9,502,175 Circuit device
60) 8,975,150 Semiconductor device manufacturing method
59) 8,823,174 Electronic device
58) 8,830,694 Circuit device
57) 8,704,355 Semiconductor device comprising through-electrode interconnect
56) 8,685,796 Electronic device and method of manufacturing the same
55) 8,633,591 Electronic device
54) 8,552,570 Wiring board, semiconductor device, and method for manufacturing wiring board and semiconductor device
53) 8,536,691 Semiconductor device and method for manufacturing the same
52) 8,456,019 Semiconductor package and method of manufacturing the same
51) 8,456,019 Semiconductor device
50) 8,436,468 Semiconductor device having a through electrode
49) 8,395,269 Method of stacking semiconductor chips including forming an interconnect member and a through electrode
48) 8,354,340 Electronic device and method of manufacturing the same
47) 8,310,039 Semiconductor device
46) 8,304,915 Semiconductor device and method for manufacturing the same
45) 8,183,685 Semiconductor device
44) 8,143,716 Semiconductor device with plate-shaped component
43) 8,115,312 Semiconductor device having a through electrode
42) 8,114,766 Method for manufacturing semiconductor device
41) 8,102,049 Semiconductor device including through electrode and method of manufacturing the same
40) 8,085,549 Circuit device
39) 8,072,073 Semiconductor device and method of manufacturing the same
38) 8,058,165 Semiconductor device and method of manufacturing the same
37) 8,035,231 Semiconductor device and method of manufacturing the same
36) 8,035,217 Semiconductor device and method for manufacturing same
35) 8,030,201 Semiconductor device and method of manufacturing the same
34) 8,022,529 Semiconductor device and method of manufacturing the same
33) 8,008,191 Semiconductor device and method of manufacturing the same
32) 7,999,401 Semiconductor device and method of manufacturing same
31) 7,928,001 Electronic device and method of manufacturing the same
30) 7,927,999 Method of forming metal interconnect layers for flip chip device
29) 7,898,073 Semiconductor device and semiconductor module employing thereof
28) 7,892,973 Method for manufacturing a semiconductor device
27) 7,807,567 Semiconductor device with interconnection structure for reducing stress migration
26) 7,800,233 Semiconductor device and method of manufacturing the same
25) 7,768,133 Semiconductor device and semiconductor module employing thereof
24) 7,759,786 Electronic circuit chip, and electronic circuit device and method for manufacturing the same
23) 7,656,046 Semiconductor device
22) 7,652,375 Semiconductor device and method of manufacturing the same
21) 7,633,167 Semiconductor device and method for manufacturing same
20) 7,598,590 Semiconductor chip and method for manufacturing the same and semiconductor device
19) 7,598,117 Method for manufacturing semiconductor module using interconnection structure
18) 7,541,677 Semiconductor device comprising through-electrode interconnect
17) 7,538,022 Method of manufacturing electronic circuit device
16) 7,528,068 Method for manufacturing semiconductor device
15) 7,495,345 Semiconductor device-composing substrate and semiconductor device
14) 7,405,472 Semiconductor device
13) 7,262,486 SOI substrate and method for manufacturing the same
12) 7,247,935 Semiconductor device
11) 7,145,247 Offset-bonded, multi-chip semiconductor device
10) 7,033,928 Method of fabricating semiconductor device
9) 6,881,666 Method of fabricating semiconductor device
8) 6,437,331 Bolometer type infrared sensor with material having hysteresis
7) 6,205,658 Method for formation of metal wiring
6) 6,048,632 Self-biasing, non-magnetic, giant magnetoresistance sensor
5) 5,759,266 Method for growing a CdTe layer on a Si substrate by a molecular beam epitaxy
4) 5,696,655 Self-biasing non-magnetic giant magnetoresistance
3) 5,581,117 Si base substrate covered by a CdTe or Cd-rich CdZnTe layer
2) 5,574,958 Hydrogen radical producing apparatus
1) 5,477,809 Method of growth of CdTe on silicon by molecular beam epitaxy

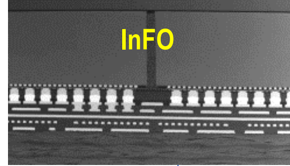
**Licensed: 4 patents**

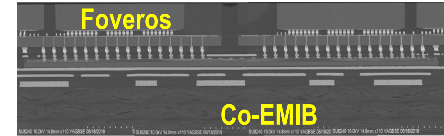
**Awarded: 1 patent**
**“NEC Most Valuable Patent in 1995”**

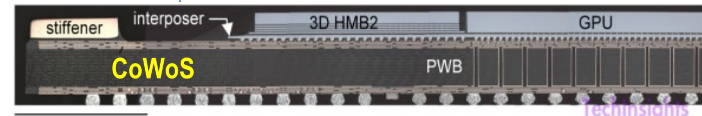
# Chip-to-Wafer Hybrid Bonding

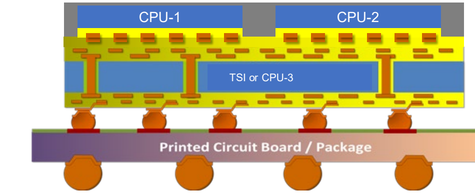
| Wiring Density IO/mm$^2$ | 100 | 200 | 400 ~ 1000 | ≥2500 |
|---|---|---|---|---|
| Pitch/um | 100 (C4) | 70 (CuP) | 50 ~ 30 (CuP) | ≤20 (Hybrid Bond) |









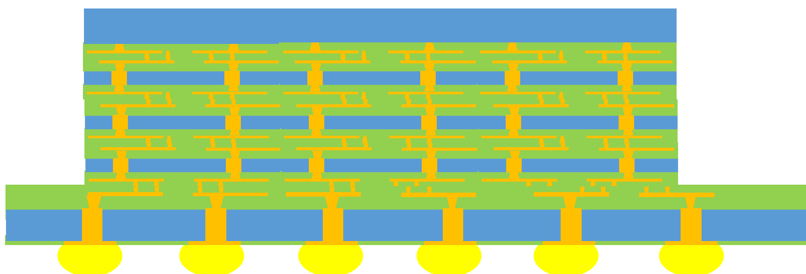



Target: **4-layer ≤10um pitch C2W-HB process development and demonstration**

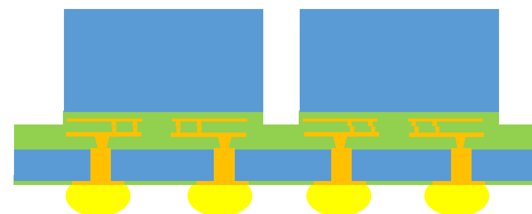
Key process challenges

- CMP (<10nm Cu dishing and <0.5nm dielectric surface roughness)
- Dielectric material evaluation for high yield hybrid bonding
- In-situ plasma cleaning / surface activation
- Particle-less assembly process (Dicing→Dice pick-up→Plasma cleaning→Bonding)

**4-layer 3D memory hybrid bonding**



**2.5D/3D hybrid bonding**



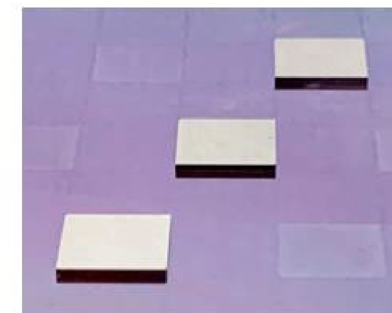


Figure 1. C2W Hybrid Bonding

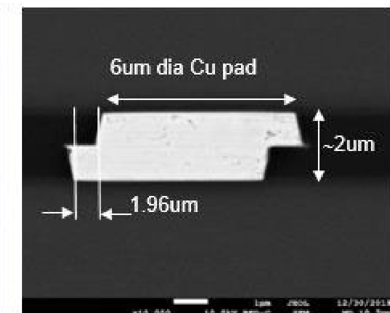



Figure 2. Cross section of C2W Hybrid Bonding

https://www.a-star.edu.sg/docs/librariesprovider18/default-document-library/ctw-consortium_media-factsheet_15feb-final.pdf

# Wafer-to-Wafer Hybrid Bonding

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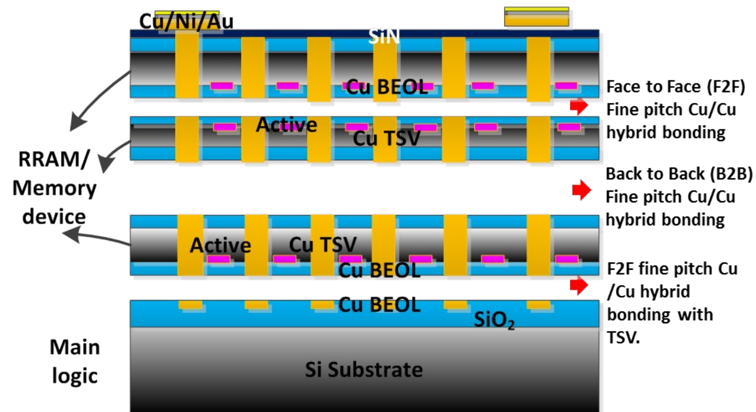
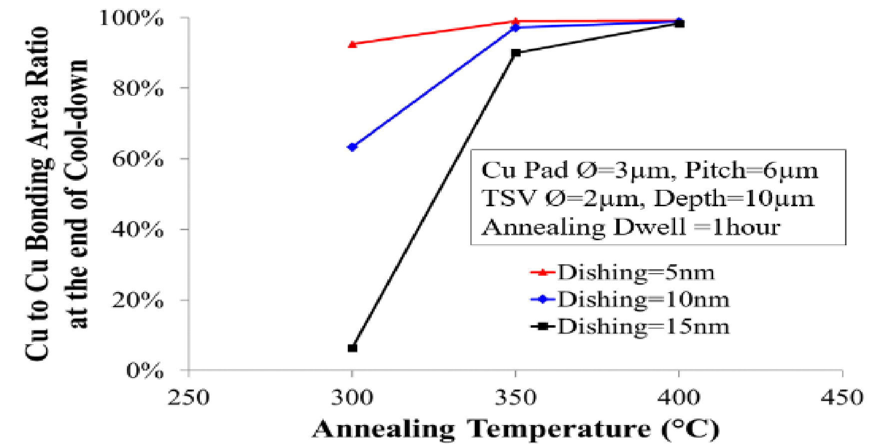
d.lab Systems Design Lab
RaaS




**Target: 4-layer wafer stack by hybrid bonding**

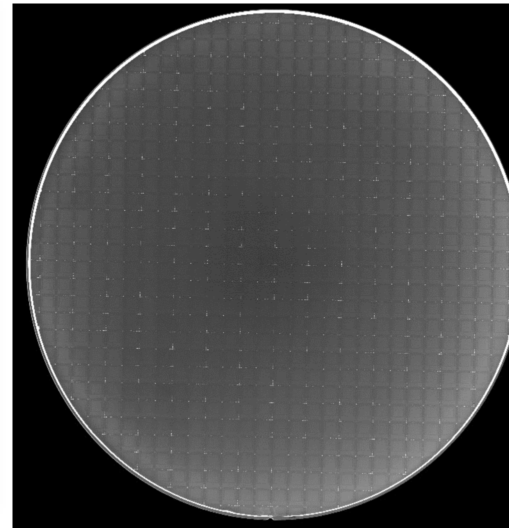


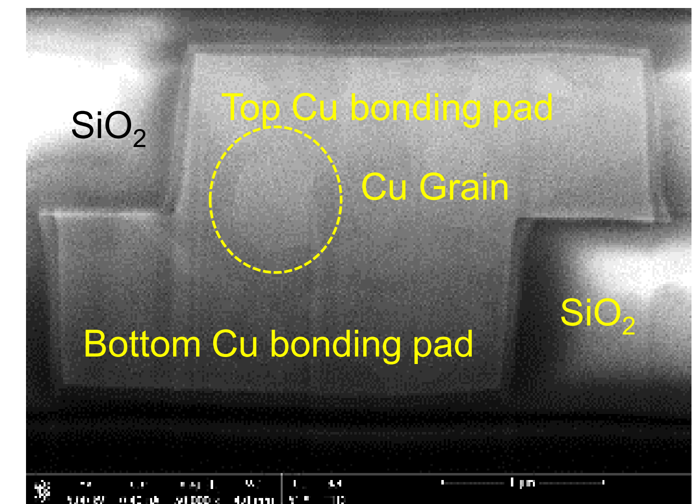

**Effect of annealing temperature and dishing value**

*Ji Lin et al., ECTC 2020*

Key development items:

- CVD optimization for high bond strength (> 1.6 $J/m^2$)
- Precise Cu dishing control (<10nm) by multi-step CMP
- Surface roughness control (<0.5nm) of dielectric layer
- Pre-bond treatment for surface activation and Cu oxide reduction
- Backgrind optimization for back-to-back direct bonding
- Edge-trim process to minimize wafer edge chipping during subsequent process steps



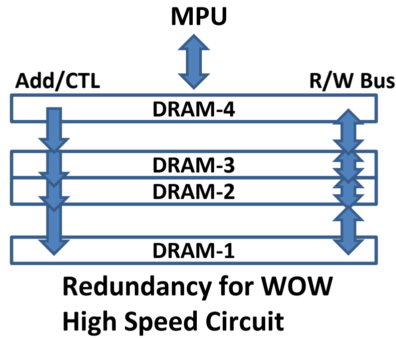



**CSAM image and XSEM after W2W hybrid bonding**

*Li Hongyu et al., EPTC 2021*

# One-step TSV for cost-effective 3D stacked DRAM

## 1. Circuit



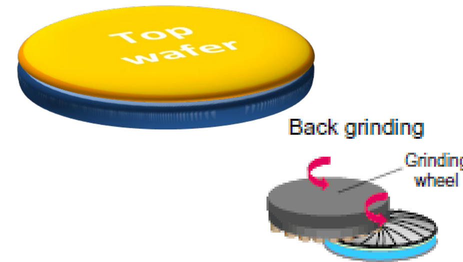

Redundancy for WOW
High Speed Circuit

## 2. F2F Bonding

Face-to-face wafer bonding (2-stack)

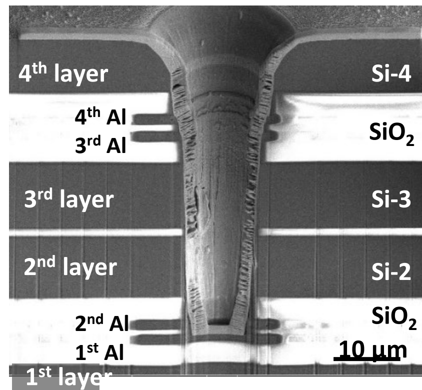
## 3. Top wafer thinning and CMP

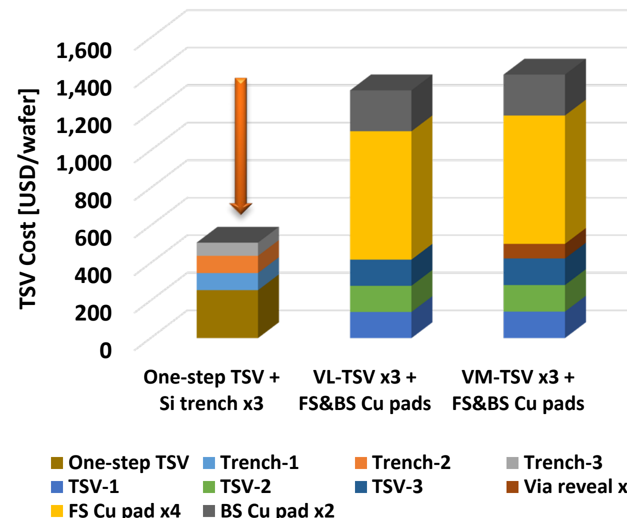
Si thickness: $\leq$ 10µm
Surface roughness: < 0.5nm



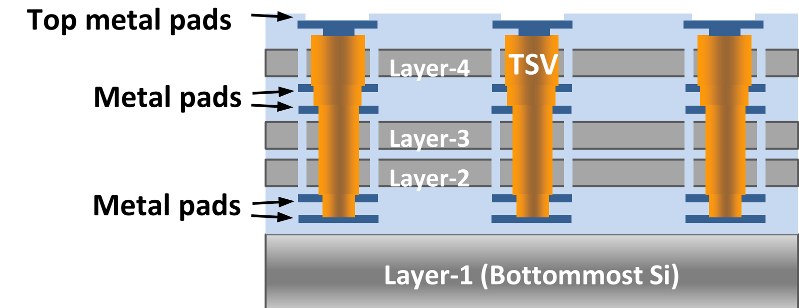

## 4. B2B Bonding

Back-to-back multi-wafer stacking (4-stack)




## 5. One-step TSV after multi-wafer stacking




More than 50% cost reduction is possible by adopting one-step TSV after multiple wafer stacking

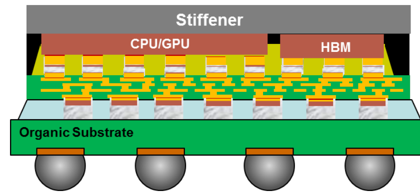
*M. Kawano et al., ECTC 2019-2022*

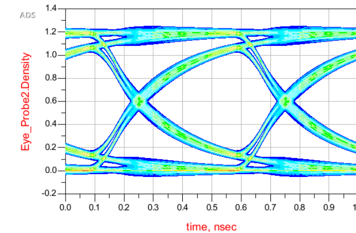
# High Density TSV-Free Interposer (TFI) Packaging with Submicron Cu Damascene RDLs for Integration of CPU/GPU and HBM

IEEE ELECTRONICS PACKAGING SOCIETY
ECTC
The 2018 IEEE 68th Electronic Components and Technology Conference

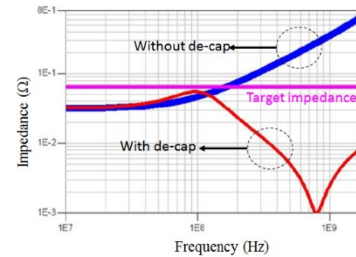
## Description

- Integrating thick HBM modules (~400µm) in TFI package increases risk of warpage issue.
- Cu-damascene RDLs have weakness on high frequency transmission and power integrity.
- Thin RDLs (5µm) can easily be damaged especially at debonding step.
- Si carrier will be eventually wasted. Glass is not compatible with damascene process.

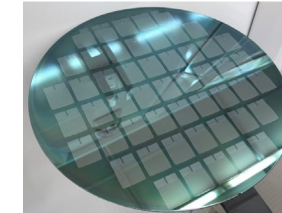


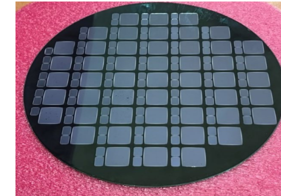



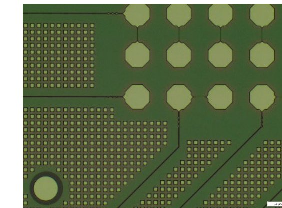

2Gbps eye pattern for crosstalk analysis



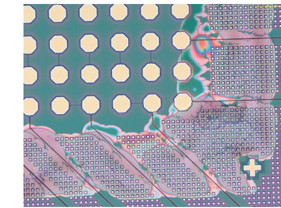

Effect of de-cap (40nF) on RDL impedance







a) Acid base etch

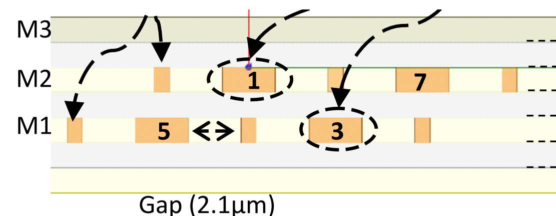


b) TMAH base etch

Si carrier removal by 2 types of etchants

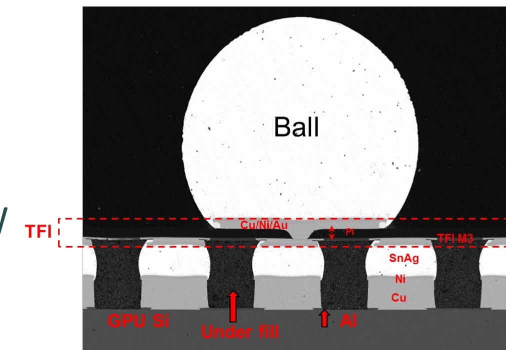
## Approach

- Package design optimized by mechanical/electrical simulations.
- Control warpage < 1mm throughout the process by concurrent design and < 250µm at a critical step by warpage correction.
- Si carrier removal process is evaluated with different types of Si wet etchant.
- Glass carrier debonding with laser-lift off method is developed which enables carrier recycle.




## Conclusion

- TFI package which can accommodate CPU/GPU and HBM modules was successfully demonstrated.
- 2Gbps with 6mm line length and 100W power distribution capabilities were confirmed by SI/PI simulation.
- Damage-less Si carrier removal was demonstrated by acid base Si etch.
- Glass carrier debonding process was developed for further cost reduction.

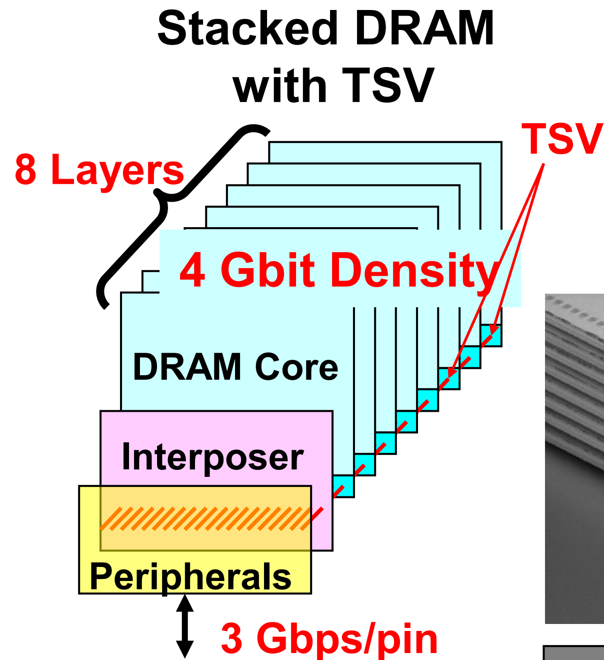


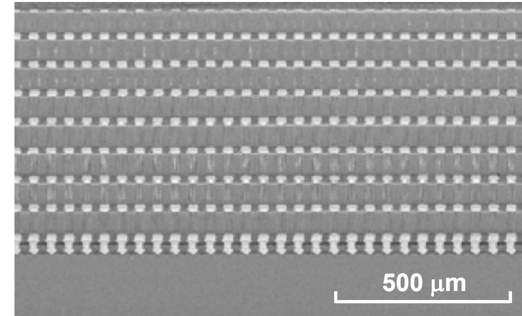
Institute of Microelectronics
A*STAR

# Word's first demonstration of Stacked DRAM with TSV

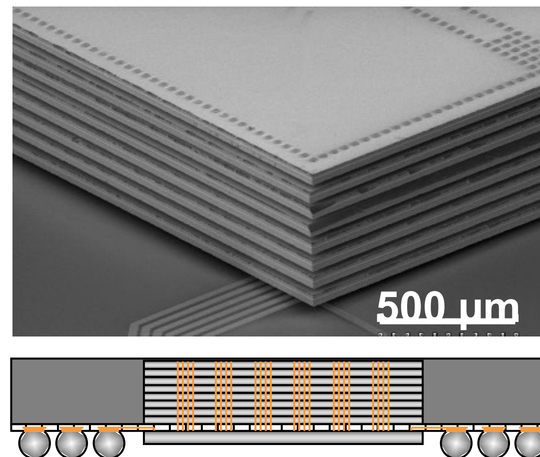
***Elpida, Oki, and NEC-EL have jointly developed 3D-DRAM with poly-Si TSVs from 2004 to 2007.***

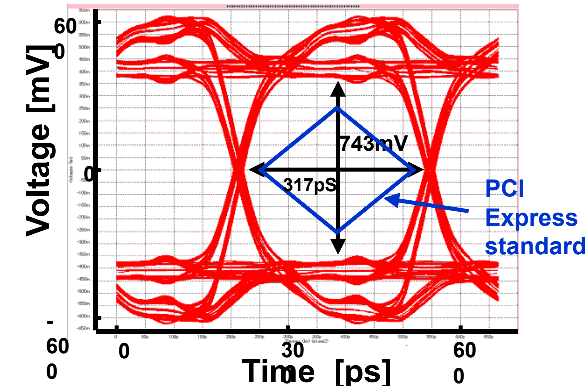
( Supported by NEDO)




TSV Interconnection
Material: Poly-Si
Pitch: 50 μm
Bump counts: 1560




Input: 3 Gbps random pulse
Frequency: 200 MHz ~ 10 GHz

**Eight stacked 4Gb DRAM with poly-Si TSVs;**
**Device performances have been fully evaluated.**

*M. Kawano et al., T-ED 55 (2008)*

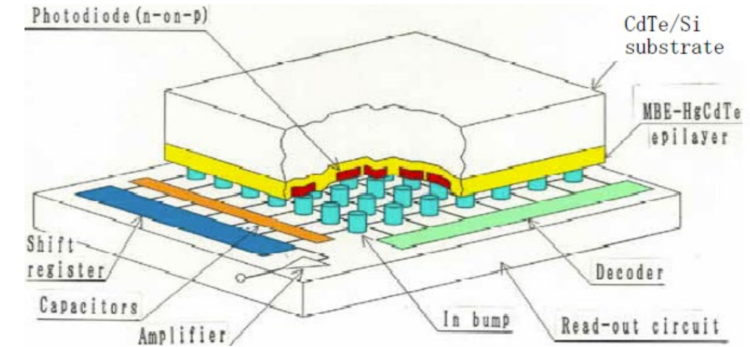
# Backside Illuminated HgCdTe/Si Infrared Image Sensor

## Purposes of research

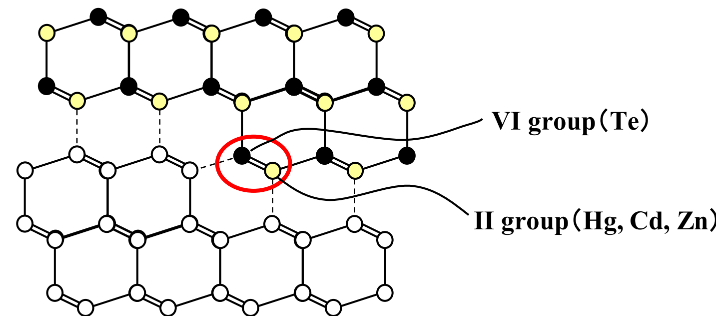
- To obtain high quality HgCdTe on Si, which enables Si-CMOS stack as well as large area.
- To realize high-pixel (256x256) IR image sensors on HgCdTe/Si

## Original achievements

1. Established precise control of molecular beam and substrate temperature.
2. Discovered the best orientation for HgCdTe growth→ $(\bar{1}\bar{1}\bar{2})$B
3. Succeeded to grow HgCdTe$(\bar{1}\bar{1}\bar{3})$B on Si(112)5°off by unique growth technique.
4. Succeeded to fabricate high-pixel (256x256) HgCdTe/Si IR image sensors.



MBE grown HgCdTe surface on 3 inch Si wafer.
Mirro-like surface morphology was obtained.

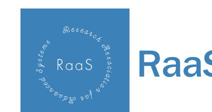



II group species do not stick to Si. If Te sticks on Si terrace, A-surface of HgCdTe will be grown, and it is difficult to obtain single crystal.

Under excess Zn irradiation, Zn bonds with Te at a step resulting "B surface" growth.

256x256 HgCdTe/Si IR sensor image

*M. Kawano et al., JCG 117 (1992) 171／M. Kawano et al., JEM 24 (1995) 431／M. Kawano et al., APL 69 (1996) 2876.*




# Thank You!

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